CS385 – Final Report

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# Introduction

# Architecture

**Description –**

**Single Cycle Datapath–**

# Instruction Set

|  |  |  |
| --- | --- | --- |
| **Instruction Set** | | **Instruction Format** |
| add | 0000 | |  |  |  |  |  | | --- | --- | --- | --- | --- | | op | rs | rt | rd | Unused | | 4 | 2 | 2 | 2 | 6 | |
| sub | 0001 |
| and | 0010 |
| or | 0011 |
| slt | 0111 |
| addi | 0100 | |  |  |  |  | | --- | --- | --- | --- | | op | rs | rt | value / address | | 4 | 2 | 2 | 8 | |
| sw | 0110 |
| lw | 0101 |
| beq | 1000 | |  |  | | --- | --- | | op | address | | 4 | 12 | |
| bne | 1001 |

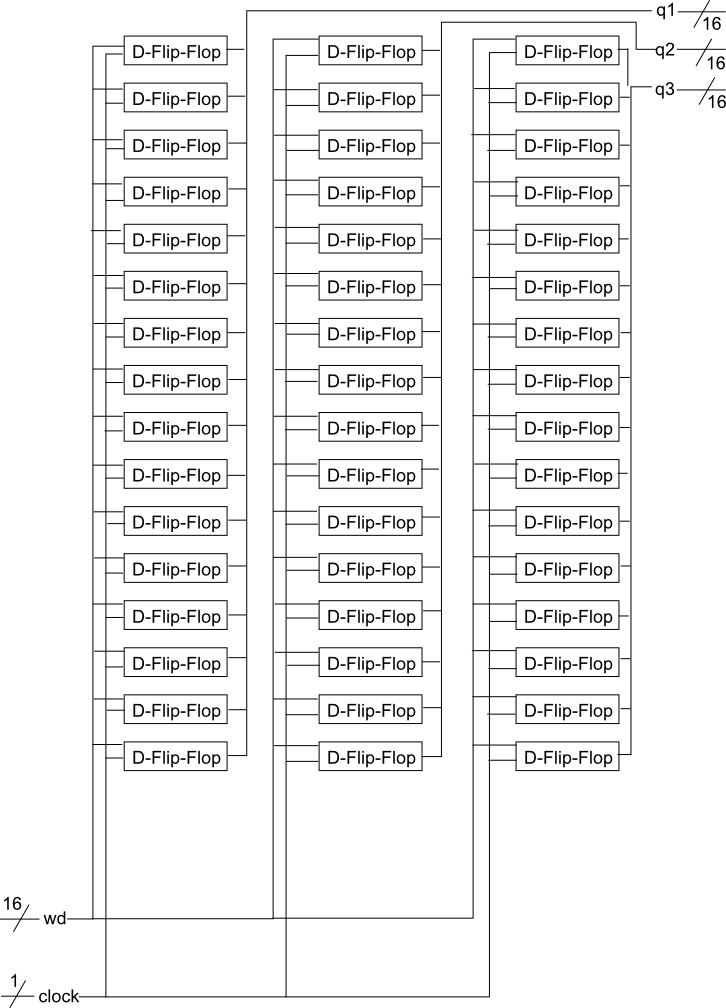
# Components

## Registers

**Description –** Registers store and maintain data for use between each clock pulse cycle. They are used both in reading data and for writing back into registers for future use. Because of this, they are one of the few pieces of the CPU utilized in multiple cycles and is more prone to hazards in a pipelined data path.

This CPU design utilizes a 16-bit D-flip-flop architecture for register storage and retrieval. This is achieved by chaining together 1-bit D-flip-flops on a negative edge change. Additionally, each D-flip-flop is actually pieced together from two D-latchs.

**Diagram –**

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**Excitation Table(s) –**

## Instruction / Data Memory

**Description –**

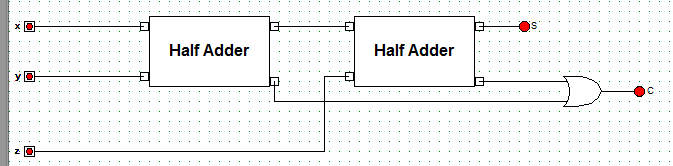
## ALU

**Description –** The Arithmetic Logic Unit, or ALU, is the workhorse of the CPU producing the results of different operations – with the exception of branch and memory instructions. Depending upon the Opcode it may produce several different instructions with the supplied register data.

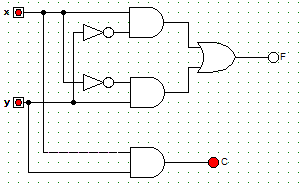
This CPU uses a 16-bit ALU built upon a hierarchical style. The 16-bit ALU is built upon 16, 1-bit ALU’s (including a special most significant bit ALU). Those 1 bit ALU’s are made using a full-adder that in turn is made up of half-adders.

**Diagram –**

Full Adder



Half Adder



**Truth Table(s) –**

Half Adder

|  |  |  |  |
| --- | --- | --- | --- |
| x | y | C | S |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

## Pipelines

**Description –**

**Diagram –**

## Multiplexers

**Description –**

**Diagram –**

**Truth Table(s) –**

# Program

# Simulation Results